IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2822
Examiner: David GRAYBILL

In Re PATENT APPLICATION Of:
Applicant : Mitsuru KOMIYAMA and Shinsuke Suzuki

Serial No. : 09/963,590

Filed : September 27, 2001

For : MULTI-CHIP PACKAGE TYPE SEMICONDCUTOR DEVICE

Attorney Ref.: F00ED0023

APPEAL BRIEF

March 1, 2006

Commissioner for Patents
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Sir:

INTRODUCTION

This is an Appeal to the Board of patent Appeals and Interferences from the decision in the Office Action dated July 1, 2005, finally rejecting claims 1, 2, 5-7, 11, 13-17, 19-23, 30, 32, 34 and 36-42. Together with a Petition for a three-month extension, ARGUMENTS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW was filed with a Notice of Appeal on December 28, 2005. On February 3, 2006, the Notice of Panel Decision from Pre-Appeal Brief Review was mailed, maintaining the rejection of claims mentioned above. Accordingly, it is respectfully submitted that the present Appeal Brief is timely.

A fee of $ 500.00 under 37 C.F.R. 41.20 (b)(2) is being submitted concurrently. Should any fee be further needed, please charge it to our Account No. 50-0945 and notify us accordingly.

(i) REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Oki Electric Industry Co., Ltd.

(ii) RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of the undersigned agent, there are no prior or pending appeals, interferences, or judicial proceedings which my be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

(iii) STATUS OF CLAIMS

Claims 1, 2, 5-7, 11, 13-17, 19-23, 30, 32, 34 and 36-42 are pending in this application. They all stand finally rejected by the examiner, and the rejection was maintained by the Panel of Pre-appeal Brief Review. Claims 3, 4, 8-10, 12, 18, 24-29, 31, 33, 35 have been cancelled. No claims are allowed.

(iv) STATUS OF AMENDMENTS

No amendment has been filed after the Final Rejection.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The present application is direct to a multi-chip package type semiconductor device. The characteristics of each independent claim are described as follows.

(a) Independent Claim 1

Fig. 2A would be a best drawing to represent the invention claimed in claim 1. A multi-chip package type semiconductor device claimed in claim 1 includes an insulating substrate, a first semiconductor device (3) and a second semiconductor device (5) formed on the first semiconductor chip (3). The insulating substrate includes a first conductive pattern (6a) and a second conductive pattern (6b) on its surface.

The first important characteristic is that the first semiconductor chip (3) includes, a plurality of first terminal pads (11a) and a plurality of conductive relay pads (11b), wherein each first terminal pad (11a) and each conductive relay pad (11b) are alternatively aligned.

The second important characteristic is how to connect the second semiconductor chip (5) to the second conductive pattern (6b). Although the first important characteristic is a common character through all independent claims, the second important characteristic is slightly different from each other. In claim 1, the first semiconductor chip (3) has the

conductive relay pads (11b) including a first area (X) and a second area (Y), which is different from the first area, wherein a first metal bump (15) is formed on the conductive relay pads (11b) in the first area (X). The second semiconductor chip (5) has a second terminal pad (13) on which a second metal bump (16) is formed. In order to connect the second semiconductor chip (5) to the second conductive pattern (6b), one end of a second bonding wire (18a) is formed on the second conductive pattern (6b) and the other end thereof is formed at the top of the first metal bump (15) on one of the conductive relay pads (11b) in the first area (X), and one end of a third bonding wire (18b) is formed on the one of the conductive relay pads (11b) in the second area (Y) and the other end is formed at the top of the second metal bump (16).

According to these characteristics described above, it is possible to secure a sufficient space between a first bonding wires (17), which connect the first terminal pad (11a) to the first conductive pattern (6a), between the second bonding wires (18a) or between the third bonding wires (18b) because each first terminal pad (11a) and each conductive relay pad (11b) are alternatively aligned. Thus, an accidental contact between the first bonding wires (17), between the second bonding wires (18a) or between the third bonding wires (18b) can be avoided.

(b) Independent Claim 13

Fig. 2A would also be a best drawing to represent the invention claimed in claim 13. The scope of claim 13 is broader than that of claim 1. While claim 1 includes further limitation that the first semiconductor chip includes an insulating substrate having thereon a first conductive pattern and a second conductive pattern, a first internal circuit, which is connected to the first terminal pad, and the second semiconductor chip includes a second internal circuit, which is connected to the second terminal pad, claim 13 does not have such limitations. Thus, it can be said that the first and second important characteristics mentioned above will meet to claim 13.

According to these characteristics described above, the benefit described above can be obtained.

(c) Independent Claim 15

Fig. 5 would be a best drawing to represent the invention claimed in claim 15. As described above, the first important characteristic is a common character through all independent claims including claim 15.

As to the second important characteristic regarding how to connect the second semiconductor chip (5) to the second conductive pattern (6b), one end of a second bonding wire (36a) is formed on one of the second conductive pattern (6b) and the other end thereof is formed at the top of one of the first metal bumps (32) formed on the conductive relay pad (31b), and one end of a third bonding wire (36b) is formed at the top of the first

metal bump (32) and the other end thereof is formed at the top of one of the second metal bumps (35) formed on the second semiconductor chip (5).

According to these characteristics described above, the benefit described above can be obtained.

(d) Independent Claim 17

Fig. 6 would be a best drawing to represent the invention claimed in claim 17. As described above, the first important characteristic is a common character through all independent claims including claim 17.

As to the second important characteristic regarding how to connect the second semiconductor chip (5) to the second conductive pattern (6b), one end of a second bonding wire (46a) is formed on the second conductive pattern (6b) and the other end thereof is formed at the top of the metal bump (42) formed on the conductive relay pad (41b), and one end of a third bonding wire (46b) is formed on the second terminal pad (44) and the other end thereof is formed at the top of the metal bump (42).

According to these characteristics described above, the benefit described above can be obtained.

(e) Independent Claim 20

Fig. 2A would be a best drawing to represent the invention claimed in claim20. This claim 20 may be a broadest claim. As described above, the first important characteristic is a common character through all independent claims including claim 20.

As to the second important characteristic regarding how to connect the second semiconductor chip (5) to the second internal terminal (6b), the claim 20 specifically focuses on the connection between the first semiconductor chip (3) and the second internal terminal (6b). That is, the first semiconductor chip (3) is connected to the second internal terminal (6b) by a wire (18a), whose one end is formed on the second internal terminal (6b) and the other end is formed at the top of the bump (15), which is formed on the second conductive portions (11b) in the second area (X).

According to these characteristics described above, it is possible to secure a sufficient space between wires because each first conductive portion and each second conductive portion are alternatively aligned.

(f) Independent Claim 37

Fig. 3 would be a best drawing to represent the invention claimed in claim 37. As described above, the first important characteristic is a common character through all independent claims including claim 37.

As to the second important characteristic regarding how to connect

the second semiconductor chip (5) to the second conductive pattern (6b), one end of a second bonding wire (23a) is formed on the second conductive pattern (6b) and the other end thereof is formed on one of the conductive relay pads (11b) in the first area (X), and one end of a third bonding wire (23b) is formed on the second terminal pad (13) formed on the second semiconductor chip (5) and the other end thereof is formed at the top of the metal bump (21) on the conductive relay pad (11b) in the second area (Y).

According to these characteristics described above, the benefit described above can be obtained.

(vi) GROUND OF REJECTION TO BE REVIEWED ON APPEAL

(a) Claim 13, 14, 19-23, 32, 36 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Takiar (U.S. patent 5, 422, 435), and Mathew (U.S. patent 5, 328, 079), or in that alternative, under 35 U.S.C. 103(a) as being unpatentable over Takiar (U.S. patent 5, 422, 435), Mathew (U.S. patent 5, 328, 079) and Fujiyama (U.S. patent 6, 148,505).

(b) Claim 1,2,5,6,7,11,15, 16,17,30,34,37-42 (are rejected under 35 U.S.C. 103 (a) as being unpatentable over Takiar (U.S. patent 5, 422, 435), and Mathew (U.S. patent 5, 328, 079), or Takiar (U.S. patent 5, 422, 435), and Mathew (U.S. patent 5, 328, 079) in combination with any of Haba (U.S. patent 6, 376,904) and Fujiyama (U.S. patent 6, 148,505).

(vii) ARGUMENT

(a) Regarding all claims against Takiar, Mathew, Fujiyama, and Haba or their combinations.

(1) None of the cited references disclose the following features:

① each first terminal pad and each conductive relay pad are alternatively aligned (claims 1, 13, 15, 17 and 37) or

② each first conductive portion and each second conductive portion are alternatively aligned (claim 20). [These arguments ① and ② have been made in the Paper dated 4/6/05, page 21, line 3 - page 22, line 11]

(b) Regarding claim 13,14,19-23,32,36

(1) Against Takiar:

① First Terminal Pad is not disclosed by Takiar [This argument has been made in the Paper dated 3/10/2004, page17, lines 5-8],

② Insulating substrate is not disclosed by Takiar [This argument has been made in Paper dated 3/10/2004, page17, lines 8-12], and

③ conductive relay pad including a first area and a second area is not disclosed by Takiar [This argument has been made in

Paper dated 12/16/02 attached to the Paper dated 2/11/03, page 7, lines 3-10]

(2) Against Fujiyama, Fujiyama does not disclose the following characteristics;

① a second bonding wire, wherein one end thereof is formed on the internal terminal and the other end is formed at the top of the first metal bump, and a third bonding wire, wherein one end thereof is formed on the conductive relay pad in the second area and the other end is formed at the top of the second metal bump (claim 13),

② a wire, wherein one end thereof is formed on the second internal terminal and the other end is formed at the top of the bump (claim 20),

③ a first wire, wherein one end thereof is formed on the first conductive pattern and the other end is formed at the top of the first bump; and a second wire, wherein one end thereof is formed at the top of the first bump and the other end is formed at the top of the second bump (claim 25) [These arguments ①, ② and ③ have been made in the Paper dated 8/26/2004, page 23, line 10 - page 24, line12].

④ In addition, Fujishima does not disclose a conductive relay pad and a first terminal, each of which is formed on the 1st

semiconductor chip [This argument ④ has been made in the Paper dated 3/10/2004 page18, lines10-13]

(3) Against Mathew

① Mathew does not disclosed any bumps claimed Paper dated [This argument has been made in the Paper dated 12/16/02 attached to the Paper dated 2/11/03, page 10, line 15 - page11, line 2]. By this argument, the rejection under Mathew made on October 2, 2002 regarding claims 24, 27 was withdrawn in the next Action.

(c) Regarding claims 1, 2, 5, 6, 7, 11, 15, 16,17, 30, 34 and 37-42

(1) Against Takiar

① Insulating substrate is not disclosed by Takiar [This argument has been made in the Paper dated 3/10/2004, page 19, line 20 – page 20, line 2]

② No first and second conductive pattern formed on the insulating substrate by Takiar [This argument has been made in the Paper dated 3/10/2004, page 20, lines 2 – 4]

③ The electrical Contact 32 does not connect the electrical lead 46 by any bonding wire by Takiar. (This means that the examiner asserted that an electrical contact 32 corresponds to the first terminal pad 32. If so, the electrical contact 32 should be connected to the electrical lead 46 by a bonding wire. But, The

electrical Contact 32 does not connect the electrical lead 46 by any bonding wire) [This argument has been made in the Paper dated 3/10/2004, page 20, lines 4 - 5]

④ A conductive relay pad including a first area and a second area is not disclosed by Takiar [This argument has been made in the Paper dated 12/16/02 attached to the Paper dated 2/11/03, page 7, line 17 – page 8, line 17]

(2) Against Fujiyama does not disclose the following characteristics;

① a second bonding, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of the first metal bump on the conductive relay pad in the first area; and a third bonding wire, wherein one end thereof is formed on the conductive relay pad in the second area and the other end is formed at the top of the second metal bump (claim 1),

② a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of the first metal bump, and a third bonding wire, wherein one end thereof is formed at the top of the first metal bump and the other end is formed at the top of the second metal bump (claim 15).

③ In addition, Fujishima does not disclose a conductive relay pad and a first terminal, each of which is formed on the 1st

semiconductor chip [These arguments ①, ② and ③ have been made in the Paper dated 3/10/2004, page 20, lines10-13])

(3) Against Haba

① The bonding wire 440a does not correspond to the first bonding wire of the invention by Haba [These argument has been made in the Paper dated 12/16/02 attached to the Paper dated 2/11/03, page 9, lines 9-19]

② A conductive relay pad including a first area and a second area is not disclosed by Haba [This argument has been made in the Paper dated 12/16/02 attached to the Paper dated 2/11/03 page 9, lines 19-20]

(4) Against Mathew

① Mathew does not disclosed any bumps claimed [This argument has been made in the Paper dated 12/16/02 attached to the Paper dated 2/11/03, page 10, line 15 - page11, line 2]. By this argument, the rejection under Mathew made on October 2, 2002 regarding claims 24, 27 was withdrawn in the next Action.

(d) Conclusion

(1) Since none of the reference cited during the prosecution disclose the characteristics (a)(1)①&② described above, all pending claims should be allowable.

(2) Further, the examiner asserts some elements, which are not expressly disclosed in the primary reference, are disclosed in the secondary reference. However, as described above in (b) and (c), Applicant argued that some elements are not still disclosed in the secondary references by showing the reasons in Papers. Since the examiner could not explain why Applicant's argument is wrong and why the undisclosed elements are disclosed, the examiner should accept the Applicant's argument.

Respectfully submitted

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(viii) CLAIMS APPENDIX

The claim involved in this appeal are presented below:

Claim 1: A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a plurality of first internal circuits on the insulating substrate, the first semiconductor chip having a plurality of first terminal pads, each of which is connected to one of the first internal circuits and a plurality of conductive relay pads, each of which is isolated from the first terminal pads, and each of the conductive relay pads including a first area and a second area, which is different from the first area, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of first metal bumps, each of which is formed on one of the conductive relay pads in the first area;

a second metal bump formed on the second terminal pad;

a first bonding wire, wherein one end thereof is formed on one of the first terminal pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of the first metal bump on one of the conductive relay pads in the first area; and

a third bonding wire, wherein one end thereof is formed on the one of the conductive relay pads in the second area and the other end is formed at the top of the second metal bump,

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 2: A multi-chip package type semiconductor device, as claimed in claim 1, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claims 3 and 4 (cancelled).

Claim 5: A multi-chip package type semiconductor device, as claimed in claim 2, wherein each of the conductive relay pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side

of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 6: A multi-chip package type semiconductor device, as claimed in claim 2, wherein one of the conductive relay relay pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 7: A multi-chip package type semiconductor device, as claimed in claim 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claims 8-10 (cancelled).

Claim 11: A multi-chip package type semiconductor device, as claimed in claim 2, wherein the first metal bump is spaced apart from the one end of the third bonding wire, but is electrically connected to the one end of the third bonding wire via the conductive relay pad.

Claim 12 (cancelled).

Claim 13 (currently amended): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a plurality of first terminal pads and a plurality of conductive relay pads, each of the conductive relay pads including a first area and a second area, which is different from the first area, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to one of the conductive relay pads in the second area;

a plurality of first metal bumps, each of which is formed on one of the conductive relay pads in the first area;

a second metal bump formed on the second terminal pad;

a first internal terminal connected to one of the first terminal pads;

a second internal terminal connected to one of the conductive relay pads in the first area;

a first bonding wire, wherein one end thereof is formed on the first internal terminal and the other end is formed on one of the first terminal pads;

a second bonding wire, wherein one end thereof is formed on the second internal terminal and the other end is formed at the top of the first metal bump formed on one of the conductive relay pads; and

a third bonding wire, wherein one end thereof is formed on the one of the conductive relay pads in the second area and the other end is formed at the top of the second metal bump.

Claim 14: A multi-chip package type semiconductor device, as claimed in claim 13, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 15: A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a plurality of first internal circuits, a plurality of first terminal pads, each of which is connected to one of the first internal circuits and a plurality of conductive relay pads, each of which is isolated from the first terminal pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of first metal bumps, each of which is formed on one of the conductive relay pads;

a second metal bump formed on the second terminal pad;

a first bonding wire, wherein one end thereof is formed on one of the first terminal pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of one of the first metal bumps; and

a third bonding wire, wherein one end thereof is formed at the top of the one of the first metal bumps and the other end is formed at the top of the second metal bump;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 16 (original): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 17: A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a plurality of first internal circuits, a plurality of first terminal pads, each of which is connected to one of the first internal circuits and a plurality of conductive relay pads, each of which is isolated from the first terminal pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of metal bumps, each of which is formed on one of the conductive relay pads;

a first bonding wire, wherein one end thereof is formed on one of the first terminal pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of one of the metal bumps; and

a third bonding wire, wherein one end thereof is formed on the second terminal pad and the other end is formed at the top of the one of the metal bumps;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 18 (cancelled).

Claim 19: A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 20: A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a plurality of first conductive portions and a plurality of second conductive portions, each of which has a first area and a second area, which is different from the first area, wherein each first conductive portion and each second conductive portion are alternatively aligned;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to one of the second conductive portion in the first area;

a plurality of bumps, each of which is formed on one of the second conductive portions in the second area;

a first internal terminal connected to one of the first conductive portions;

a second internal terminal connected to one of the second conductive portions in the second area; and

a wire, wherein one end thereof is formed on the second internal terminal and the other end is formed at the top of the one of the bumps.

Claim 21: A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 22: A multi-chip package type semiconductor device, as claimed in claim 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 23: A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are spaced from each other.

Claims 24-29 (cancelled).

Claim 30: A multi-chip package type semiconductor device, as claimed in claim 1, wherein each of the first terminal pads is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claims 31 (cancelled).

Claim 32: A multi-chip package type semiconductor device, as claimed in claim 13, wherein each of the first terminal pads is rectangularly-shaped, and a side of the first terminal pad is parallel to a side of the first semiconductor chip.

Claims 33 (cancelled).

Claim 34: A multi-chip package type semiconductor device, as claimed in claim 15, wherein each of the first terminal pads is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claims 35 (cancelled).

Claim 36: A multi-chip package type semiconductor device, as claimed in claim 20, wherein each of the first conductive portions is rectangularly-shaped, and a side of the first conductive portion is parallel to a side of the first semiconductor chip.

Claim 37: A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a plurality of first internal circuits on the insulating substrate, the first semiconductor chip having a plurality of first terminal pads, each of which is connected to one of the first internal circuits and a plurality of conductive relay pads, each of which is isolated from the first terminal pads, and each of which includes a first area and a second area, which is different from the first area, each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of metal bumps, each of which is formed on one of the conductive relay pads in the second area;

a first bonding wire, wherein one end thereof is formed on one of the first terminal pads and the other end is formed on the first conductive pattern;

a second bonding, wherein one end thereof is formed on the second conductive pattern and the other end is formed on one of the conductive relay pads in the first area; and

a third bonding wire, wherein one end thereof is formed on the second terminal pad and the other end is formed at the top of the metal bump on the one of the conductive relay pads in the second area;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 38: A multi-chip package type semiconductor device, as claimed in claim 37, wherein the second semiconductor chip is placed on the center of the first semiconductor chip

Claim 39: A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the conductive relay pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side

of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 40: A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the conductive relay pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 41: A multi-chip package type semiconductor device, as claimed in claim 40, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 42: A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the metal bumps is spaced apart from the one end of the second bonding wire, but is electrically connected to the one end of the second bonding wire via the conductive relay pad.

(ix) EVIDENCE APPENDIX

No new evidence is being submitted with this brief.

(x) RELATED PROCEEDING APPENDIX

In view of Section (ii) of this Brief, no copies of decision are appended.

IFW 2822

PTO/SB/17 (01-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500

Complete if Known	
Application Number	09/963,590
Filing Date	September 27, 2001
First Named Inventor	Mitsuru KOMIYAMA
Examiner Name	David GRAYBILL
Art Unit	2822
Attorney Docket No.	F00ED0023

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0945 Deposit Account Name: Oki America, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)	Fee Paid ($)
_____	- 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)	Fee Paid ($)
_____	- 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
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